REMARKS

These comments are responsive to the Official Action mailed on Office Action mailed on December 31, 2003. Claims 63-77 and 80-124 are currently pending. The Office Action notes that claims 63-77 and 80-106 have been copied and requires support to be provided for particular elements of the claims, additionally rejecting claims 63-77 and 80-124 under 35 U.S.C. 112, first paragraph. Additionally, claims 63-77 and 80-93 are rejected under 35 U.S.C. 102(e) as anticipated by Banks (6,014,327) and Banks (6,344,998). These topics are all addressed under the appropriate heading below.

Additionally, the Office Action objected to the disclosure due an informality in claim 104. Claim 104 has been amended in order to correct its dependency. The Applicants thank the Examiner for noting this error. The other pending claims are all as previously submitted.

Support for Claims 63-77 and 80-106

Applicants have previously supplied support for all of the pending claims in the Amendment of September 9, 2003, submitted in response to the previous Office Action. This previous Amendment provided support in a two-column format; although the Applicants believe that the previous Amendment presented sufficient support, the present Amendment provides further detail for those specific elements where the Office Action feels more explanation is required.

More specifically, the Office Action states: "For example, for claim 63, Applicant must point out where in the specification the channels of multi-level cells are being coupled between the bit line and the reference potential, or what are the verifying reference parameters and the reading reference parameters are. Applicant directed to Figures 11c, 11d, 15a, 15b of Patent '344, but did not specifically point out each element or limitation."

For "channels of multi-level cells are being coupled between the bit line and the reference potential":

The cells shown as T_{10}, T_{11}, etc. in Figure 15a of '344 and 500a, 500b, etc. in Figure 15b of '344. In Figure 15a, these are connected between ground (a reference potential) and the bit lines connected to V_{D0}, V_{D1}, etc. Figure 15b is a virtual ground array with the cells connected between two bit lines, the connection to the reference potential being through one

of the bit lines, where the values are given in Figure 17b. The Office Action is correct in that these figures do not explicitly show the channel. The channel region is explicitly shown in the many schematic figures of cells shown in the earlier figures of '344; for example, see Figure 5a where the channel of cell 500a is indicated by reference numbers 520a and 512a.

Also see Figure 12 of the present application, which shows cells 63, 65, ..., again connected in a virtual ground array between bit lines 91, 93, ..., through which the cell is connected on one side to a reference potential whose values are given in Figures 26 and 27. The channel is shown explicitly in Figure 9, where it is indicated by L1 and L2.

For the "verifying reference parameters":

These are shown in Figure 11c of the '344 patent (which is also Figure 15B of the present application). These are the reference current $I_{REF("3")}$, $I_{REF("2")}$, $I_{REF("1")}$, and $I_{REF("0")}$, which are used as is described at column 26, lines 4-50, of '344, where the emphasis is added:

> ... For a four state storage, four sense amplifiers, each with its own distinct current reference levels IREF,0, IREF,1, IREF,2, and IREF,3 are attached to each decoded output of the bit line. ....
>
> *During programming*, the four data inputs Ii (I0, I1, I2 and I3) are presented to a comparator circuit which also has presented to it the four sense amp outputs for the accessed cell. If Di match Ii, then the cell is in the correct state and no programming is required. If however all four Di do not match all four Ii, then the comparator output activates a programming control circuit. This circuit in turn controls the bit line (VPBL) and word line (VPWL) programming pulse generators. A single short programming pulse is applied to both the selected word line and the selected bit line. This is followed by a second read cycle to determine if a match between Di and Ii has been established. This sequence is repeated through multiple programming/reading pulses and is stopped only when a match is established (or earlier if no match has been established but after a preset maximum number of pulses has been reached).
>
> The result of such multistate programming algorithim is that each cell is programmed into any one of the four conduction states in direct correlation with the reference conduction states I_{REF}, i. ...

For the "reading reference parameters":

These are also shown in Figure 11c of the '344 patent (which is also Figure 15B of the present application). These are again the reference current $I_{REF("2")}$, $I_{REF("1")}$, and $I_{REF("0")}$, which are used as is described at column 26, lines 4-18, of '344, except that for the

embodiment to which the present claims are drawn, for the read process these are shifted with respect to their values as programming reference parameters so that they are arranged as described in the claim. This is described at 26, lines 51-65, of `344, where the emphasis is added:

> In actual fact, although four reference levels and four sense amplifiers are used to program the cell into one of four distinct conduction states, only three sense amplifiers and three reference levels are required to sense the correct one of four stored states. For example, in FIG. 11c, I sub REF ("2") can differentiate correctly between conduction states "3" and "2", I sub REF ("1") can differentiate correctly between conduction states "2" and "1", and I sub REF ("0") can differentiate correctly between conduction states "1" and "0". *In a practical implementation of the circuit of FIG. 11e the reference levels I sub REF, i (i=0,1,2) may be somewhat shifted by a fixed amount <u>during sensing</u> to place them closer to the midpoint between the corresponding lower and higher conduction states of the cell being sensed.*

Consequently, the three reading reference parameters are placed between the four programming parameters as described in the manner described in the claims.

<u>Rejections under 35 U.S.C. 112, first paragraph</u>

The Office Action has rejected claims 63-77, 80-93, and 94-124 all under 35 U.S.C. 112, first paragraph, due to lack of support for the verifying reference parameters and for these parameters not being related to the reading reference parameters as described in the claims. This has been addressed in the preceding section, where support for these elements is given.

Claims 94-124 are also rejected under 35 U.S.C. 112, first paragraph, as failing to provide an adequate written description for the parameter generating circuitry. In a particular embodiment of the present invention, these parameters are various reference currents that are provided by reference cells. In various embodiments, these reference cells are shown as 431, 433, 435 in Figure 17B; as MASTER REF. CELLS 507 in Figure 18; in Figure 20A as 523, 525, 529; in Figure 21A as 523, 525, 531; in Figure 21 as 551, 553, 555; and in Figure 21C. These circuits are described in detail in the section of the material included by the Preliminary Amendment filed concurrently with the present application entitled "Read Circuits and Techniques Using Reference Cells" which begins on page 9, line 19, of the Preliminary Amendment.

Consequently, it is therefore respectfully submitted that the rejections under 35 U.S.C. 112, first paragraph, are not well founded and should be withdrawn.

Rejections under 35 U.S.C. 102(e)

The Office Action rejected claims 63-77 and 80-93 are rejected under 35 U.S.C. 102(e) as anticipated by Banks (6,014,327) and Banks (6,344,998), from which a number of the pending claims have been taken. As specified in the "Cross-Reference to Related Application" section added to the beginning of the present application by Preliminary Amendment filed concurrently with the present application, and as is also shown on the filing receipt, the present application is entitled to an effective filing date of April 13, 1989.

U.S. patent 6,344,998 of Banks has a filing date of February 28, 2001, and claiming priority from a number of U.S. patent applications, the earliest of which has a filing date of February 8, 1991. Thus, this earliest priority date is well over a year after the effective filing date of the present application.

Similarly, U.S. patent 6,014,327 of Banks has a filing date of May 14, 1999, and claiming priority from a number of U.S. patent applications (in one case through a continuation in-part), the earliest of which has a filing date of February 8, 1991. Thus, again this earliest possible priority date is well over a year after the effective filing date of the present application.

Consequently, it is therefore respectfully submitted that the rejection claims 63-77 and 80-93 under 35 U.S.C. 102(e) is not well founded and should be withdrawn.

Conclusion

An early examination and allowance of the present application are solicited, and if there are any questions about the support provided above and in the previous response, a call to the undersigned is invited.

Respectfully submitted,

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